Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

M.E DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2025

Second Semester

Power Systems Engineering

PPST2421-Advanced Power System Protection

Regulations – 2024

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Identify a real-time condition where numerical relays outperform electromechanical ones in protection speed.	L2	1	2
2.	Indicate two specific applications of the sampling theorem in numerical relay-based power system protection.	L2	1	2
3.	Identify a function of distance relays that contributes to fault discrimination in Extra High Voltage (EHV) systems.	L2	2	2
4.	Interpret the benefit of software-based design for digital protection in long transmission corridors.	L1	2	2
5.	Recall any two types of common faults observed in synchronous generators under abnormal system operating conditions.	L1	3	2
6.	List the major protection schemes used for synchronous generators in large thermal power stations.	L1	3	2
7.	Indicate the key features of directional multi-zone distance relays used in high voltage power networks.	L2	4	2
8.	State the basic parameters considered for distance relay zone setting.	L1	4	2
9.	List the various fault types considered during short-circuit analysis in the development of protective relay algorithms.	L1	5	2
10.	Indicate the essential input data required for developing PC-based relay setting and coordination software tools.	L2	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a i	Interpret how Least Error Squared (LES) technique contributes to reducing error during current signal reconstruction in protective algorithms.	L2	1	8
	i i	Outline the key benefits of applying the sampling theorem for accurate fault identification in fast-acting numerical relays.	L2	1	8
		Or			
	b i	Demonstrate the role of multiple processing blocks in numerical relays to ensure effective protection and rapid response under real-time conditions.	L2	1	8

		i i	Summarize the advantages of numerical protection schemes using block diagrams and explain their role in fault isolation.	L2	1	8
12.	a	i	Use distance relaying logic to isolate a fault within Zone 2, considering impedance reach settings and directionality control.	L3	2	8
		i i	Implement amplitude comparison-based logic to distinguish between forward and reverse faults in a digital protection system.	L3	2	8
			Or			
	b	i	Select appropriate software features for a microprocessor-based relay to manage high-speed faults in transmission networks.	L3	2	8
		i i	Choose relevant parameters for hardware implementation of a distance relay targeting long transmission corridors applications.	L3	2	8
13.	a	i	Analyze the limitations of traditional generator protection during unbalanced loading and suggest digital upgrades for better performance.	L4	3	8
		i i	Analyse the various faults in Synchronous Generators.	L4	3	8
			Or			
	b	i	Analyze the response of a digital relay system when a phase-to-phase fault occurs in a transformer secondary winding.	L4	3	8
		i i	Investigate the effects of varying generator operating conditions on the stability and accuracy of digital protection algorithms.	L4	3	8
14.	a	i	Explain the influence of fault impedance on zone-2 and zone-3 operation in distance relays and show its implication in setting.	L2	4	8
		i i	Identify the operational differences between multi-zone distance relays and instantaneous overcurrent relays in parallel feeder configurations.	L2	4	8
			Or			
	b		Explain the sequence of coordinated operations in an overcurrent relay using Inverse Definite Minimum Time (IDMT) characteristics under varying fault levels in detail.	L2	4	16
15.	a		A transformer substation experienced delayed fault clearance. Study the relay settings and propose adjustments using PC-based tools with necessary diagrams.	L5	5	16
			Or			
	b		Assess a real-time protection failure during a three-phase fault and construct an alternative solution using PC application-based relay logic design.	L5	5	16